FORM PTO-1449

INFORMATION DISCLOSURE STATEMENT

ATTY. DOCKET NO. SP088.C6	APPLICATION NO. 10/083,143
APPLICANT Deosaran *et al.*	
FILING DATE February 27, 2002	GROUP ~~2172~~ 2183

U.S. PATENT DOCUMENTS

EXAMINER INITIAL		DOCUMENT NUMBER	DATE	NAME	CLASS	SUB-CLASS	FILING DATE
WMT	AA1	4,626,989	12/1986	Torii	~~364~~	~~200~~	
	AB1	4,675,806	06/1987	Uchida	364	200	
	AC1	4,722,049	01/1988	Lahti	364	200	
	AD1	4,807,115	02/1989	Torng	364	200	
	AE1	4,901,233	02/1990	Liptay	364	200	
	AF1	4,903,196	02/1990	Pomerene	364	200	
	AG1	4,942,525	07/1990	Shintani *et al.*	364	200	
	AH1	4,992,938	02/1991	Cocke *et al.*	364	200	
WMT	AI1	5,067,069	11/1991	Fite *et al.*	~~395~~	~~375~~	

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EXAMINER INITIAL		DOCUMENT NUMBER	DATE	COUNTRY	CLASS	SUB-CLASS	TRANSLATION
WMT	AJ1	WO 88/09035 A2	11/1988	PCT	G11C	8/00	N/A
	AK1	WO 91/20031 A1	12/1991	PCT	G06F	9/45	N/A
	AL1	0 378 195 A2 & A3	07/1990	EP	G06F	5/06	N/A
WMT	AM1	0 515 166 A1	11/1992	EP	G06F	9/38	N/A

OTHER (Including Author, Title, Date, Pertinent Pages, etc.)

WMT	AN	1	Acosta, R. D. *et al.*, "An Instruction Issuing Approach to Enhancing Performance in Multiple Functional Unit Processors," *IEEE Transactions On Computers*, IEEE, Vol. C-35, No. 9, pp. 815-828 (September 1986).
	AO	1	Agerwala, T. and Cocke, J., "High Performance Reduced Instruction Set Processors," IBM Research Division, pp. 1-61 (March 31, 1987).
	AP	1	Aiken, A. and Nicolau, A., "Perfect Pipelining: A New Loop Parallelization Technique," *Proceedings of the 1988 ESOP*, Springer-Verlag, pp. 221-235 (1988).
	AQ	1	Charlesworth, A.E., "An Approach to Scientific Array Processing: The Architectural Design of the AP-120B/FPS-164 Family," *Computer*, IEEE, Vol. 14, pp. 18-27 (September 1981).
WMT	AR	1	Colwell, R.P. *et al.*, "A VLIW Architecture for a Trace Scheduling Compiler," *Proceedings of the 2nd International Conference on Architectural Support for Programming Languages and Operating Systems*, ACM, pp. 180-192 (October 1987).

EXAMINER	W. TRBAT	DATE CONSIDERED	9/17/04

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	APPLICANT Deosaran *et al.*	
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U.S. PATENT DOCUMENTS

EXAMINER INITIAL		DOCUMENT NUMBER	DATE	NAME	CLASS	SUB-CLASS	FILING DATE
WMT	AA2	5,072,364	12/1991	Jardine *et al.*	395	375	
	AB2	5,109,495	04/1992	Fite *et al.*	395	375	
	AC2	5,142,633	08/1992	Murray *et al.*	395	375	
	AD2	5,167,026	11/1992	Murray *et al.*	395	375	
	AE2	5,214,763	05/1993	Blaner *et al.*	395	375	
	AF2	5,222,244	06/1993	Carbine *et al.*	395	800	
	AG2	5,226,126	07/1993	McFarland *et al.*	395	375	
	AH2	5,230,068	07/1993	Van Dyke *et al.*	395	375	
WMT	AI2	5,251,306	10/1993	Tran	395	375	

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EXAMINER INITIAL		DOCUMENT NUMBER	DATE	COUNTRY	CLASS	SUB-CLASS	TRANSLATION
WMT	AJ2	0 533 337 A1	03/1993	EP	G06F	9/38	N/A
	AK2						
	AL2						
	AM2						

OTHER (Including Author, Title, Date, Pertinent Pages, etc.)

WMT	AN	2	Dwyer, H, *A Multiple, Out-of-Order Instruction Issuing System for Superscalar Processors*, UMI, pp. 1-249 (August 1991).
	AO	2	Foster, C.C. and Riseman, E.M., "Percolation of Code to Enhance Parallel Dispatching and Execution," *IEEE Transactions On Computers*, IEEE, pp. 1411-1415 (December 1971).
	AP	2	Goodman, J.R. and Hsu, W., "Code Scheduling and Register Allocation in Large Basic Blocks," *International Conference on Supercomputing*, ACM, pp. 442-452 (1988).
	AQ	2	Gross, T.R. and Hennessy, J.L., "Optimizing Delayed Branches," *Proceedings of the 5th Annual Workshop on Microprogramming*, IEEE, pp. 114-120 (October 5-7, 1982).
WMT	AR	2	Groves, R.D. and Oehler, R., "An IBM Second Generation RISC Processor Architecture," *Proceedings 1989 IEEE International Conference on Computer Design: VLSI in Computers and Processors*, IEEE, pp. 134-137 (October 1989).

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INFORMATION DISCLOSURE STATEMENT

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APPLICANT Deosaran *et al.*	
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U.S. PATENT DOCUMENTS

EXAMINER INITIAL		DOCUMENT NUMBER	DATE	NAME	CLASS	SUB-CLASS	FILING DATE
WMT	AA3	5,255,384	10/1993	Sachs *et al.*	~~395~~	~~425~~	
	AB3	5,261,071	11/1993	Lyon	395	425	
	AC3	5,278,963	01/1994	Hattersley *et al.*	395	400	
	AD3	5,317,720	05/1994	Stamm *et al.*	395	425	
	AE3	5,345,569	09/1994	Tran	395	375	
	AF3	5,355,457	10/1994	Shebanow *et al.*	395	376	
	AG3	5,371,684	12/1994	Iadonato *et al.*	395	491	
	AH3	5,398,330	03/1995	Johnson	395	575	
WMT	AI3	5,442,757	08/1995	McFarland *et al.*	395	375	

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EXAMINER INITIAL		DOCUMENT NUMBER	DATE	COUNTRY	CLASS	SUB-CLASS	TRANSLATION
	AJ3						
	AK3						
	AL3						
	AM3						

OTHER (Including Author, Title, Date, Pertinent Pages, etc.)

WMT	AN	3	Horst, R.W. *et al.*, "Multiple Instruction Issue in the NonStop Cyclone Processor," *Proceedings of the 17th Annual International Symposium on Computer Architecture*, IEEE, pp. 216-226 (1990).
	AO	3	Hwu, W-M. W. and Patt, Y.N., "Checkpoint Repair for High-Peformance Out-of-Order Execution Machines," *IEEE Trans. On Computers*, IEEE, Vol. C-36, No. 12, pp. 1496-1514 (December 1987).
	AP	3	Hwu, W-M. W. and Chang, P.P., "Exploiting Parallel Microprocessor Microarchitectures with a Compiler Code Generator," *Proceedings of the 15th Annual Symposium on Computer Architecture*, IEEE, pp. 45-53 (June 1988).
	AQ	3	Hwu, W-M. and Patt, Y.N., "HPSm, a High Performance Restricted Data Flow Architecture Having Minimal Functionality," *Proceedings from ISCA-13*, IEEE, pp. 297-306 (June 2-5, 1986).
WMT	AR	3	*IBM Journal of Research and Development*, IBM, Vol. 34, No. 1, pp. 1-70 (January 1990).

EXAMINER	DATE CONSIDERED
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EXAMINER INITIAL		DOCUMENT NUMBER	DATE	NAME	CLASS	SUB-CLASS	FILING DATE
Kent	AA4	5,448,705	09/1995	Nguyen *et al.*	~~395~~	~~375~~	
	AB4	5,487,156	01/1996	Popescu *et al.*	395	375	
	AC4	5,497,499	03/1996	Garg *et al.*	395	800	
	AD4	5,524,225	06/1996	Kranich	395	403	
	AE4	5,560,032	09/1996	Nguyen *et al.*	395	800	
	AF4	5,561,776	10/1996	Popescu *et al.*	395	375	
	AG4	5,574,927	11/1996	Scantlin	395	800	
	AH4	5,590,295	12/1996	Deosaran *et al.*	395	393	
Kent	AI4	5,592,636	01/1997	Popescu *et al.*	~~395~~	~~586~~	

FOREIGN PATENT DOCUMENTS

EXAMINER INITIAL		DOCUMENT NUMBER	DATE	COUNTRY	CLASS	SUB-CLASS	TRANSLATION
	AJ4						
	AK4						
	AL4						
	AM4						

OTHER (Including Author, Title, Date, Pertinent Pages, etc.)

Kent	AN	4	Johnson, M. *Superscalar Microprocessor Design*, Prentice-Hall, Entire book submitted (1991).
	AO	4	Johnson, W. M., *Super-Scalar Processor Design*, (Dissertation), 134 pages (1989).
	AP	4	Jouppi, N.P. and Wall, D.W., "Available Instruction-Level Parallelism for Superscalar and Superpipelined Machines," *Proceedings of the 3rd International Conference on Architectural Support for Programming Languages and Operating Systems*, ACM, pp. 272-282 (April 1989).
	AQ	4	Jouppi, N.P., "Integration and Packaging Plateaus of Processor Performance," *International Conference of Computer Design*, IEEE, pp. 229-232 (October 1989).
Kent	AR	4	Jouppi, N.P., "The Nonuniform Distribution of Instruction-Level and Machine Parallelism and Its Effect on Performance," *IEEE Transactions on Computers*, IEEE, Vol. 38, No. 12, pp. 1645-1658 (December 1989).

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U.S. PATENT DOCUMENTS

EXAMINER INITIAL		DOCUMENT NUMBER	DATE	NAME	CLASS	SUB-CLASS	FILING DATE
kemt	AA5	5,606,676	02/1997	Grochowski *et al.*	~~395~~	~~586~~	
	AB5	5,619,668	04/1997	Zaidi	395	376	
	AC5	5,625,837	04/1997	Popescu *et al.*	395	800	
	AD5	5,627,983	05/1997	Popescu *et al.*	~~395~~	393	
	AE5	5,708,841	01/1998	Popescu *et al.*	~~395~~	800	
	AF5	5,737,624	04/1998	Garg *et al.*	395	800.23	
	AG5	5,768,575	06/1998	McFarland *et al.*	395	569	
	AH5	5,778,210	07/1998	Henstrom *et al.*	~~395~~	394	
kemt	AI5	5,797,025	08/1998	Popescu *et al.*	~~395~~	~~800~~	

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EXAMINER INITIAL		DOCUMENT NUMBER	DATE	COUNTRY	CLASS	SUB-CLASS	TRANSLATION
	AJ5						
	AK5						
	AL5						
	AM5						

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kemt	AN	5	Keller, R.M., "Look-Ahead Processors," *Computing Surveys*, ACM, Vol. 7, No. 4, pp. 177-195 (December 1975).
	AO	5	Lam, M.S., "Instruction Scheduling For Superscalar Architectures," *Annu. Rev. Comput. Sci.*, Annual Reviews, Vol. 4, pp. 173-201 (1990).
	AP	5	Lightner, B.D. and Hill, G., "The Metaflow Lightning Chipset", *Compcon Spring 91*, IEEE, pp. 13-18 (February 25 - March 1, 1991).
	AQ	5	Murakami, K. *et al.*, "SIMP (Single Instruction stream/Multiple instruction Pipelining): A Novel High-Speed Single-Processor Architecture," *Proc. 16th Int. Symp. on Computer Architecture*, ACM, pp.78-85 (June 1989).
kemt	AR	5	Patt, Y.N. *et al.*, "Critical Issues Regarding HPS, A High Performance Microarchitecture", *Proceedings of 18th Annual Workshop on Microprogramming*, IEEE, pp. 109-116 (December 3-6, 1985).

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U.S. PATENT DOCUMENTS

EXAMINER INITIAL		DOCUMENT NUMBER	DATE	NAME	CLASS	SUB-CLASS	FILING DATE
WM	AA6	5,809,276	09/1998	Deosaran *et al.*	~~395~~	~~393~~	
	AB6	5,832,205	11/1998	Kelly *et al.*	395	185.06	
	AC6	5,832,293	11/1998	Popescu *et al.*	395	~~800.23~~	
	AD6	6,138,231	10/2000	Deosaran *et al.*	712	216	
WM	AE6	6,272,617 B1	08/2001	Deosaran *et al.*	~~712~~	23	
	AF6						
	AG6						
	AH6						
	AI6						

FOREIGN PATENT DOCUMENTS

EXAMINER INITIAL		DOCUMENT NUMBER	DATE	COUNTRY	CLASS	SUB-CLASS	TRANSLATION
	AJ6						
	AK6						
	AL6						
	AM6						

OTHER (Including Author, Title, Date, Pertinent Pages, etc.)

WM	AN	6	Patt, Y.N. *et al.*, "HPS, A New Microarchitecture: Rationale and Introduction", *The 18th Annual Workshop on Microprogramming*, Pacific Grove, CA, December 3-6, 1985, IEEE Computer Society Order No. 653, pp. 103-108.
	AO	6	Patterson, D.A. and Hennessy, J.L., *Computer Architecture: A Quantitative Approach*, Morgan Kaufmann Publishers, pp. 257-278, 290-314 and 449 (1990).
	AP	6	Peleg, A. and Weiser, U., "Future Trends in Microprocessors: Out-of-Order Execution, Speculative Branching and their CISC Performance Potential", IEEE, pp. 263-266 (1991).
	AQ	6	Pleszkun, A.R. and Sohi, G.S., "The Performance Potential of Multiple Functional Unit Processors," *Proceedings of the 15th Annual Symposium on Computer Architecture*, IEEE, pp. 37-44 (June 1988).
WM	AR	6	Pleszkun, A.R. *et al.*, "WISQ: A Restartable Architecture Using Qu u s," *Proceedings of the 14th International Symposium on Computer Architecture*, ACM, pp. 290-299 (June 1987).

EXAMINER	DATE CONSIDERED
Lee, TRBAT	9/17/04

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EXAMINER INITIAL		DOCUMENT NUMBER	DATE	NAME	CLASS	SUB-CLASS	FILING DATE
	AA7						
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FOREIGN PATENT DOCUMENTS

EXAMINER INITIAL		DOCUMENT NUMBER	DATE	COUNTRY	CLASS	SUB-CLASS	TRANSLATION
	AJ7						
	AK7						
	AL7						
	AM7						

OTHER (Including Author, Title, Date, Pertinent Pages, etc.)

lemT	AN	7	Popescu, V. *et al.*, "The Metaflow Architecture", *IEEE Micro*, IEEE, Vol. 11, No.3, pp. 10-13 and 63-73 (June 1991).
	AO	7	Smith, M.D. *et al.*, "Boosting Beyond Static Scheduling in a Superscalar Processor," *International Symposium on Computer Architecture*, IEEE, pp. 344-354 (May 1990).
	AP	7	Smith, J.E. and Pleszkun, A.R., "Implementation of Precise Interrupts in Pipelined Processors," *Proceedings of the 12th Annual International Symposium on Computer Architecture*, IEEE, pp. 36-44 (June 1985).
	AQ	7	Smith, M.D. *et al.*, "Limits on Multiple Instruction Issue," *Computer Architecture News*, ACM, No. 2, pp. 290-302 (April 3-6, 1989).
lemT	AR	7	Sohi, G.S. and Vajapeyam, G.S., "Instruction Issue Logic For High-Performance, Interruptable Pipelined Processors," *Conference Proceedings of the 14th Annual International Symposium on Computer Architecture*, pp. 27-34 (June 2-5, 1987).

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M. TR EAT	9/17/04

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EXAMINER INITIAL		DOCUMENT NUMBER	DATE	NAME	CLASS	SUB-CLASS	FILING DATE
	AA8						
	AB8						
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FOREIGN PATENT DOCUMENTS

EXAMINER INITIAL		DOCUMENT NUMBER	DATE	COUNTRY	CLASS	SUB-CLASS	TRANSLATION
	AJ8						
	AK8						
	AL8						
	AM8						

OTHER (Including Author, Title, Date, Pertinent Pages, etc.)

WMT	AN	8	Thornton, J.E., *Design of a Computer: The Control Data 6600*, Control Data Corporation, pp. 58-140 (1970).
	AO	8	Tjaden, G.S. and Flynn, M.J., "Detection and Parallel Execution of Independent Instructions," *IEEE Trans. On Computers*, IEEE, Vol. C-19, No. 10, pp. 889-895 (October 1970).
	AP	8	Tjaden, G.S and Flynn, M.J. *Representation and Detection of Concurrency Using Ordering Matrices*, (Dissertation), UMI, pp. 1-199 (1972).
	AQ	8	Tjaden *et al.*, "Representation of Concurrency with Ordering Matrices," *IEEE Transactions On Computers*, IEEE, Vol. C-22, No. 8, pp. 752-761 (August 1973).
WMT	AR	8	Tomasulo, R.M., "An Efficient Algorithm for Exploiting Multiple Arithmetic Units," *IBM Journal*, IBM, Vol. 11, pp. 25-33 (January 1967).

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U.S. PATENT DOCUMENTS

EXAMINER INITIAL		DOCUMENT NUMBER	DATE	NAME	CLASS	SUB-CLASS	FILING DATE
	AA9						
	AB9						
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FOREIGN PATENT DOCUMENTS

EXAMINER INITIAL		DOCUMENT NUMBER	DATE	COUNTRY	CLASS	SUB-CLASS	TRANSLATION
	AJ9						
	AK9						
	AL9						
	AM9						

OTHER (Including Author, Title, Date, Pertinent Pages, etc.)

DEMT	AN	9	Uht, A.K., "An Efficient Hardware Algorithm to Extract Concurrency From General-Purpose Code," *Proceedings of the 19th Annual Hawaii International Conference on System Sciences*, HICSS, pp. 41-50 (1986).
	AO	9	Wedig, R.G., *Detection of Concurrency In Directly Executed Language Instruction Streams*, (Dissertation), UMI, pp. 1-179 (June 1982).
	AP	9	Weiss, S. and Smith, J.E., "Instruction Issue Logic in Pipelined Supercomputers," *IEEE Trans. on Computers*, IEEE, Vol. C-33, No. 11, pp. 1013-1022 (November 1984).
	AQ	9	Butler, M. and Patt, Y.,"An Improved Area-Efficient Register Alias Table for Implementing HPS," University of Michigan, Ann Arbor, Michigan, 24 pages (January 23, 1990).
DEMT	AR	9	Butler, M. and Patt, Y., "An Investigation of the Performance of Various Dynamic Scheduling Techniques," *Proceedings from MICRO-25*, pp. 1-9 (December 1-4, 1992).

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Ms. TRAN	9/17/04

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FORM PTO-1449

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U.S. PATENT DOCUMENTS

EXAMINER INITIAL		DOCUMENT NUMBER	DATE	NAME	CLASS	SUB-CLASS	FILING DATE
	AA10						
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EXAMINER INITIAL		DOCUMENT NUMBER	DATE	COUNTRY	CLASS	SUB-CLASS	TRANSLATION
	AJ10						
	AK10						
	AL10						
	AM10						

OTHER (Including Author, Title, Date, Pertinent Pages, etc.)

WMT	AN	10	Butler, M. *et al.*, "Single Instruction Stream Parallelism Is Greater than Two," *The 18th Annual International Symposium on Computer Architecture*, ACM SIGARCH, Vol. 19, No. 3, pp. 276-286 (May 1991).
	AO	10	Gee, J. *et al.*, "The Implementation of Prolog via VAX 8600 Microcode," IEEE, pp. 68-74 (1986).
	AP	10	Hwu, W.-M. *et al.*, "An HPS Implementation of VAX: Initial Design and Analysis," *Proceedings of the Nineteenth Annual Hawaii International Conference on System Sciences*, pp. 282-291 (1986).
	AQ	10	Hwu, W.-M. *et al.*, "Design Choices for the HPSm Microprocessor Chip," *Proceedings of the Twentieth Annual Hawaii International Conference on System Sciences*, pp. 330-336 (1987).
WMT	AR	10	Hwu, W.-M. and Patt, Y.N., "HPSm2: A Refined Single-Chip Microengine," *HICSS '88*, pp. 30-40, 1988.

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	AA11						
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	AJ11						
	AK11						
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	AM11						

OTHER (Including Author, Title, Date, Pertinent Pages, etc.)

MONT	AN	11	Kateveris, Hardware Support "Thesis," pg. 138-145 (1984).
	AO	11	Melvin, S. and Patt, Y., "Exploiting Fine-Grained Parallelism Through a Combination of Hardware and Software Techniques," *The 18th Annual International Symposium on Computer Architecture*, ACM SIGARCH, Vol. 19, No. 3, pp. 287-296 (May 1991).
	AP	11	Patt, Y. *et al.*, "Experiments with HPS, A Restricted Data Flow Microarchitecture for High Performance Computers," IEEE, pp. 254-258 (1986).
	AQ	11	Patt, Y.N. *et al.*, "Run-Time Generation of HPS Microinstructions From a VAX Instruction Stream," IEEE, pp. 75-81 (October 1986).
MONT	AR	11	Swensen, J.A. and Patt, Y.N., "Hierarchical Registers for Scientific Computers," *Conference Proceedings: 1988 International Conference on Supercomputing*, ACM, pp. 346-353 (July 4-8, 1988).

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EXAMINER INITIAL		DOCUMENT NUMBER	DATE	NAME	CLASS	SUB-CLASS	FILING DATE
	AA12						
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	AD12						
	AE12						
	AF12						
	AG12						
	AH12						
	AI12						

FOREIGN PATENT DOCUMENTS

EXAMINER INITIAL		DOCUMENT NUMBER	DATE	COUNTRY	CLASS	SUB-CLASS	TRANSLATION
	AJ12						
	AK12						
	AL12						
	AM12						

OTHER (Including Author, Title, Date, Pertinent Pages, etc.)

WEAT	AN	12	Uvieghara, G.A. *et al.*, "An Experimental Single-Chip Data Flow CPU," *Symposium on ULSI Circuits Design Digest of Technical Papers*, 2 pages (May 1990).
WEAT	AO	12	Uvieghara, G.A. *et al.*, "An Experimental Single-Chip Data Flow CPU," *IEEE Journal of Solid-State Circuits*, IEEE, Vol. 27, No. 1, pp. 17-28 (January 1992).
WEAT	AP	12	Wilson, J.E. *et al.*, "On Tuning the Microarchitecture of an HPS Implementation of the VAX," *Proceedings of the 20th Annual Workshop on Microprogramming*, IEEE Computer Society, pp. 162-167 (December 1-4, 1987).
	AQ	12	
	AR	12	

EXAMINER	W. TRAT	DATE CONSIDERED	9/17/04

EXAMINER: Initial if ref rence considered, whether or not citation is in conformance with MPEP 609. Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to Applicant.